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APPLICATION

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TITLE: **CURRENT CROWDING REDUCTION TECHNIQUE USING SELECTIVE CURRENT INJECTION**

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CURRENT CROWDING REDUCTION TECHNIQUE USING SELECTIVE CURRENT INJECTION

Background of Invention

[0001] A typical computer system includes at least a microprocessor and some form of memory. The microprocessor has, among other components, arithmetic, logic, and control circuitry that interpret and execute instructions necessary for the operation and use of the computer system. Figure 1 shows a typical computer system (10) having a microprocessor (12), memory (14), integrated circuits (16) that have various functionalities, and communication paths (18), i.e., buses and wires, that are necessary for the transfer of data among the aforementioned components in the computer system (10).

[0002] An integrated circuit, such as the ones shown in Figure 1, is electrically connected to a circuit board via a chip package. A chip package, which houses semiconductor devices in strong, thermally stable, hermetically sealed environments, provides a semiconductor device, e.g., the integrated circuit, with electrical connectivity to circuitry external to the semiconductor device. Figure 2 shows one prior art type of chip package assembly that involves wire bond connections. The wire bonding process involves mounting a integrated circuit (30) to a substrate (32) with its inactive backside (34) down. Wires (not shown) are then bonded between an active side (36) of the integrated circuit (30) and the chip package (not shown).

[0003] Figure 3 shows a more recently developed type of chip package assembly known as "flip-chip" packaging. In flip-chip package technology, an integrated circuit (40) is mounted onto a chip package (42), where the active side of the integrated circuit (40) is electrically interfaced to the chip package (42). Specifically, the integrated circuit (40) has bumps (44) on bond pads (not shown

and also known and referred to as "landing pads") formed on an active side (46) of the integrated circuit (40), where the bumps (44) are used as electrical and mechanical connectors. The integrated circuit (40) is inverted and bonded to chip package (42) by means of the bumps (44). Various materials, such as conductive polymers and metals (referred to as "solder bumps"), are commonly used to form the bumps (44) on the integrated circuit (40).

[0004] As discussed above with reference to Figure 3, the bumps (44) on the integrated circuit (40) serve as electrical pathways between the components within the integrated circuit (40) and the chip package (42). Within the integrated circuit (40) itself, an arrangement of conductive pathways and metal layers form a means by which elements in the integrated circuit (40) operatively connect to the bumps (44) on the outside of the integrated circuit (40). To this end, Figure 4a shows a side view of the integrated circuit (40). The integrated circuit (40) has several metal layers, M1-M8, surrounded by some dielectric material (48), e.g., silicon dioxide. The metal layers, M1-M8, are connected to each other by conductive pathways (50) known as "vias." Vias (50) are essentially holes within the dielectric material (48) that have been doped with metal ions.

[0005] Circuitry (not shown) embedded on a substrate of the integrated circuit (40) transmit and receive signals via the metal layers, M1-M8, and the vias (50). Signals that need to be transmitted/received to/from components external to the integrated circuit (40) are propagated through the metal layers, M1-M8, and vias (50) to the top metal layer, M8. The top metal layer, M8, then transmits/receives signals and power to/from the bumps (44) located on the active side of the integrated circuit (40).

[0006] Figure 4b shows a top view of the integrated circuit (40) shown in Figure 4a. The top metal layer, M8, as shown in Figure 4b, has a number of parallel regions. These parallel regions alternate between regions connected to V_{DD} and

regions connected to V_{SS}. Such a configuration helps reduce electromagnetic interference. The top metal layer, M8, is configured such that it is orthogonal with the metal layer below, M7, as shown in Figure 4b. Further, bumps (44) on the top metal layer, M8, are arranged in a non-uniform fashion with some areas of the top metal layer, M8, having larger numbers of bumps (44) than other areas.

Summary of Invention

[0007] According to one aspect of the present invention, a bump and vias structure comprises a metal layer; a bump mounted on the metal layer; a first plurality of vias disposed on a first outer region of the metal layer, where the first outer region has a first density of vias; and a second plurality of vias disposed on a second outer region of the metal layer, where the second outer region has a second density of vias; and where the first density and second density are greater than a third density of vias disposed on a central region between the first and second outer regions.

[0008] According to another aspect, an integrated circuit comprises a metal layer; a bump mounted on the metal layer; a first plurality of vias disposed on a first outer region of the metal layer, where the first outer region has a first density of vias; and a second plurality of vias disposed on a second outer region of the metal layer, where the second outer region has a second density of vias; and where the first density and second density are greater than a third density of vias disposed on a central region between the first and second outer regions.

[0009] According to another aspect, a method for reducing current crowding in a bump and vias structure comprises distributing current from a first outer region of a metal layer to a bump mounted on the metal layer, where the first outer region has a first density of vias; and distributing current from a second outer region of the metal layer to the bump, where the second outer region has a second density of

vias, and where the first density and second density are greater than a third density of vias disposed in a central region between the first and second outer regions.

[0010] According to another aspect, a method for reducing current crowding on a bump comprises defining a first region and a second region on a metal layer to which the bump is mounted; determining a first current path length from the first region to the bump; determining a second current path length from the second region to the bump; disposing a first plurality of vias in the first region at a first density depending on the first current path length; and selectively disposing a second plurality of vias in the second region at a second density depending on the second current path length.

[0011] Other aspects and advantages of the invention will be apparent from the following description and the appended claims.

Brief Description of Drawings

[0012] Figure 1 shows a typical computer system.

[0013] Figure 2 shows a typical chip package assembly.

[0014] Figure 3 shows a typical flip-chip package assembly.

[0015] Figure 4a shows a view of a typical integrated circuit.

[0016] Figure 4b shows another view of the typical integrated circuit shown in Figure 4a.

[0017] Figure 4c shows an enlarged view of a bump and vias structure in accordance with the examples shown in Figures 4a and 4b.

[0018] Figure 5a shows a top view of a bump and vias structure in accordance with an embodiment of the present invention.

[0019] Figure 5b shows a top view of a bump and vias structure in accordance with the embodiment shown in Figure 5a.

[0020] Figure 6a shows a top view of a bump and vias structure in accordance with another embodiment of the present invention.

[0021] Figure 6b shows a top view of a bump and vias structure in accordance with the embodiment shown in Figure 6a.

[0022] Figure 7a shows a top view of a bump and vias structure in accordance with another embodiment of the present invention.

[0023] Figure 7b shows a top view of a bump and vias structure in accordance with the embodiment shown in Figure 7a.

Detailed Description

[0024] Detailed exemplary embodiments of the present invention will now be described with reference to the accompanying figures. Embodiments of the present invention are related to a bump and vias structure that allows for increased uniformity of current distribution around the bump. Embodiments of the present invention further relate to a method for reducing current crowding by more uniformly distributing current to and from a bump.

[0025] Figure 4c shows an enlarged section of the integrated circuit (40) shown in Figure 4b. Although a section of an integrated circuit is used for this example, the invention is equally applicable to all bump and vias structures in an integrated circuit. The bump (44) shown in Figure 4c is connected to the top metal layer, M8. Vias (50) are used to connect the bump (44), the top metal layer, M8, and the one or more metal layers below (shown here as layer M7).

[0026] Vias (50) provide current paths across the junction between the bump (44) and the top metal layer, M8. The part of the top metal layer, M8, that makes contact with the bump is known as its "landing pad" (52). Thus, current is carried to or from the bump (44) from or to the vias (50) by layer M8 and the landing pad (52). Arrows indicating the flow of current from the bump (44) to the vias (50)

are shown for illustration purposes in Figure 4c. Although the vias (50) facilitate current flow, because the vias (50) are positioned laterally across the layer M8, and the bump (44) is circular, there is non-uniform current density at the junction between the bump (44) and the top metal layer, M8. This non-uniform current density, resulting from the differences in current path length from the vias (50) to the bump (44), is known as "current crowding." In this current crowding phenomenon, there is high current density at a region (54) of the bump (44) that is in closest proximity to the vias (50), and there is lower current density in the rest of the junction between the bump (44) and the landing pad (52). For example, in Figure 4c, it can be seen that the shortest current path length is along arrow (55a), resulting in current crowding in region (54). A lower concentration of current flow occurs along arrows (55b), and an even lower concentration of current flow occurs along arrows (55c). Those skilled in the art will note that in Figure 4c, the relative thicknesses among arrows from the vias (50) to the bump (44) are indicative of the relative current densities of the various current flow paths. For example, arrow (55a) has a higher current density than arrows (55c), and thus arrow (55a) is thicker than arrows (55c).

[0027] Current crowding is typically an undesirable effect because prolonged exposure to current crowding may cause, among other things, performance degradation, power distribution deficiencies, signal delay, and damage to the junction between the bump (44) and the landing pad (52). In some cases, damage caused by electro-migration may actually result in detachment of the bump.

[0028] Figure 5a shows a top view of a bump and vias structure in accordance with an embodiment of the invention. In the prior art example shown in Figure 4c, current crowding occurred due to the current concentration along the central current flow path, i.e., arrow (55a). In the embodiment shown in Figure 5a, the vias (50) have been separated into vias (50a) in a first outer region (57a) and vias (50b) in a second outer region (57b). In this embodiment, the vias have been

removed from a central region (57) in between the first and second outer regions (57a and 57b), and have been concentrated along the outer regions (57a and 57b) of layer M8. Thus, vias (50a) cause a concentration of current to flow along arrow (55a), while vias (50b) cause a concentration of current to flow along arrow (55b). Because of the relative lack of current sources, i.e., vias, in the central region (57c), it can be seen that the current path lengths from the vias (50a and 50b) to the bump (44) are all virtually the same. Accordingly, current uniformity at the bump (44) is increased. Correspondingly, current crowding, and the resulting performance degradation, are decreased.

[0029] Figure 5b shows a top view of a bump and vias structure in accordance with the embodiment shown in Figure 5a. In Figure 5b, current distribution to the bump (44) is shown where vias are positioned on the metal layer, M8, on both sides of the bump (44). Current to the bump flows from the outer regions (57a) and (57b), as shown by arrows (55a and 55b), and because of the lack of vias in the central region (57c), it can be seen that the current path lengths from the vias (50a and 50b) to the bump (44) are all substantially the same. Thus, as shown in Figure 5b, the bump (44) experiences substantially uniform current distribution from the vias, effectively reducing current crowding at isolated points of the bump (44).

[0030] Turning now to Figure 6a, an alternative embodiment of the present invention is shown. In this embodiment, in addition to a relatively dense distribution of vias within the outer regions (57a and 57b) of layer M8, vias (50c) are disposed in the central region (57c), but are disposed more sparsely than vias (50a and 50b) in the outer regions (57a and 57b). Thus, by virtue of a lesser density of current flowing toward the bump (44) from the central region (57c) than current flowing from toward the bump (44) from the outer regions (57a and 57b), the differences in current path length to the bump (44) are compensated for by the differences in current injection. Accordingly, current crowding at the bump (44) is

reduced.

[0031] Figure 6b shows a top view of a bump and vias structure in accordance with the embodiment shown in Figure 6a. In Figure 6b, current distribution to the bump (44) is shown where vias are positioned on the metal layer, M8, on both sides of the bump (44). Because outer regions (57a and 57b) have higher via density than the central regions (57c) of the metal layer, M8, higher current flow densities from the outer regions (57a and 57b) to the bump (44) compensate for the longer current flow paths (arrows 55a and 55b) from the outer regions (57a and 57b) to the bump (44) relative to that of current flow path from the central region (57c) to the bump (44). Thus, as shown in Figure 6b, the bump (44) experiences substantially uniform current distribution, effectively reducing current crowding at isolated points of the bump (44).

[0032] Turning now to Figure 7a, an alternative embodiment of the present invention is shown. In this embodiment, in addition to a relatively dense distribution of vias within the outer regions (57a and 57b) of layer M8, vias (50c) are disposed in the central region (57c), but are disposed more sparsely than vias (50a and 50b) in the outer regions (57a and 57b), where the central region (57c) is positioned further away from the bump (44) than the outer regions (57a and 57b). Thus, by virtue of a lesser density of current flowing toward the bump (44) from the central region (57c) than current flowing from toward the bump (44) from the outer regions (57a and 57b), and by virtue of the central region (57c) being disposed further from the bump (44) than the outer regions (57a and 57b), the differences in current path length to the bump (44) are compensated for by the differences in current injection. Accordingly, current crowding at the bump (44) is reduced.

[0033] Figure 7b shows a top view of a bump and vias structure in accordance with the embodiment shown in Figure 7a. In Figure 7b, current distribution to the

bump (44) is shown where vias are positioned on the metal layer, M8, on both sides of the bump (44). Because outer regions (57a, 57b) have higher via density than the central regions (57c) of the metal layer, M8, and because the central region (57c) is disposed further from the bump (44) than the outer regions (57a and 57b), the differences in current path lengths to the bump (44) are compensated for by the differences in current injection. Thus, as shown in Figure 7b, the bump (44) experiences substantially uniform current distribution, effectively reducing current crowding at isolated points of the bump (44).

[0034] Although, in the exemplary embodiments above, current is shown as flowing from the vias to the bump, the invention is equally applicable for situations where current flows from the bump to the vias.

[0035] In the exemplary embodiments above, it has been shown that current uniformity at the bump can be increased, and current crowding decreased, by selectively injecting current from desired regions of a metal layer to a bump. In the examples above, these regions have been described as the outer regions (57a and 57b) of the layer M8, represented by the location of the vias (50a and 50b), and a central region (57c), represented by the location of the vias (50c). Although the metal layer, M8, has been divided into these three regions for purposes of illustration, the skilled artisan will understand that the metal layer may be divided into any number of regions, and the distribution of vias adjusted accordingly, to result in the desired distribution of current injection. Thus, the embodiments of Figures 5a thru 7b serve for illustration purposes only, and should not be considered to limit the invention.

[0036] The invention further relates to a method of reducing current crowding at a bump using selective current injection. In accordance with the method of the invention, a metal layer to which a bump is connected is divided into a plurality of regions. Within each of the plurality of regions, vias are then distributed at

varying densities to produce a level of current injection that compensates for differences in path length from each region to the bump.

[0037] While the invention has been shown and described above with respect to particular exemplary embodiments, the skilled artisan will recognize that various modifications and additions to the disclosed embodiments may be made without departing from the spirit and scope of the invention. Accordingly, the invention shall be considered limited only by the scope of the appended claims.